Amendments to the Specification

Please replace the paragraph beginning at page 15, line 26, with the following rewritten paragraph:

In the third embodiment, a VSS power line 51 is connected to the source terminal (power supply) of an N-type MOS transistor 22 of each of a given number of 5-transistor SRAM cells 11 arranged in the direction of a bit line BL. A drive voltage that is ΔV ~~higher~~ lower than the first voltage VSS from a first power supply 55, namely, a second voltage ~~VSS+ ΔV57~~ VSS-ΔV from a second power supply 57 is applied to the source terminal of the N-type MOS transistor 22b through the VSS power line 51 under the control of a power supply selection switch (selection circuit) 53 in "1" data write mode. In this case, the second voltage ~~VSS+ΔV~~ VSS-ΔV is set at about ~~105% to 130%~~ 95% to 70% of the first voltage VSS (the above voltage ΔV is set at about 5% to 30% of the first voltage VSS).